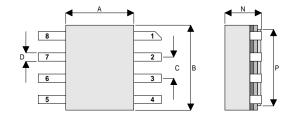
TetraFET

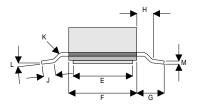
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ROHS COMPLIANT METAL GATE RF SILICON FET

MECHANICAL DATA





SO8 PACKAGE

PIN 5 – SOURCE
PIN 6 – GATE
PIN 7 – GATE
PIN 8 – SOURCE

Dim.	mm	Tol.	Inches	Tol.
Α	4.06	±0.08	0.160	±0.003
В	5.08	±0.08	0.200	±0.003
С	1.27	±0.08	0.050	±0.003
D	0.51	±0.08	0.020	±0.003
E	3.56	±0.08	0.140	±0.003
F	4.06	±0.08	0.160	±0.003
G	1.65	±0.08	0.065	±0.003
н	0.76	+0.25	0.030	+0.010
	0.70	-0.00	0.030	-0.000
J	0.51	Min.	0.020	Min.
J	1.02	Max.	0.040	Max.
K	45°	Max.	45°	Max.
L	0°	Min.	0°	Min.
-	7°	Max.	7°	Max.
М	0.20	±0.08	0.008	±0.003
Ν	2.18	Max.	0.086	Max.
Р	4.57	±0.08	0.180	±0.003

GOLD METALLISED **MULTI-PURPOSE SILICON DMOS RF FET** 10W - 12.5V - 500MHz SINGLE ENDED

FEATURES

- SIMPLIFIED AMPLIFIER DESIGN
- SUITABLE FOR BROAD BAND APPLICATIONS
- VERY LOW C_{rss}
- SIMPLE BIAS CIRCUITS
- LOW NOISE
- HIGH GAIN 10 dB MINIMUM

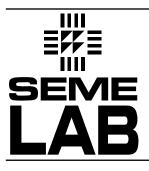
APPLICATIONS

 HF/VHF/UHF COMMUNICATIONS from 1 MHz to 1 GHz

ABSOLUTE MAXIMUM RATINGS (T_{case} = 25°C unless otherwise stated)

P _D	Power Dissipation	30W
BV _{DSS}	Drain – Source Breakdown Voltage	40V
BV _{GSS}	Gate – Source Breakdown Voltage	±20V
I _{D(sat)}	Drain Current	10A
T _{stg}	Storage Temperature	–65 to 150°C
Тj	Maximum Operating Junction Temperature	200°C

Semelab PIc reserves the right to change test conditions, parameter limits and package dimensions without notice. Information furnished by Semelab is believed to be both accurate and reliable at the time of going to press. However Semelab assumes no responsibility for any errors or omissions discovered in its use. Semelab encourages customers to verify that datasheets are current before placing orders.



ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise stated)

	Parameter	Test Conditions		Min.	Тур.	Max.	Unit
BV _{DSS}	Drain–Source Breakdown Voltage	$V_{GS} = 0$	I _D = 10mA	40			V
IDSS	Zero Gate Voltage Drain Current	V _{DS} = 12.5V	V _{GS} = 0			1	mA
I _{GSS}	Gate Leakage Current	V _{GS} = 20V	$V_{DS} = 0$			1	μΑ
V _{GS(th)}	Gate Threshold Voltage*	I _D = 10mA	$V_{DS} = V_{GS}$	1		7	V
9 _{fs}	Forward Transconductance*	V _{DS} = 10V	I _D = 1A	0.8			S
G _{PS}	Common Source Power Gain	P _O = 10W		10			dB
η	Drain Efficiency	V _{DS} = 12.5V	I _{DQ} = 0.4A	50			%
VSWR	Load Mismatch Tolerance	f = 500MHz		20:1			—
C _{iss}	Input Capacitance	$V_{DS} = 0V V_{C}$	$_{SS} = -5V f = 1MHz$			60	pF
C _{oss}	Output Capacitance	V _{DS} = 12.5V V _C	$_{\rm SS} = 0$ f = 1MHz			40	pF
C _{rss}	Reverse Transfer Capacitance	V _{DS} = 12.5V V _C	GS = 0 f = 1MHz			4	pF

* Pulse Test: Pulse Duration = 300 μs , Duty Cycle $\leq 2\%$

THERMAL DATA

R _{THi-case} Thermal F	esistance Junction – Case	Max. 6°C / W
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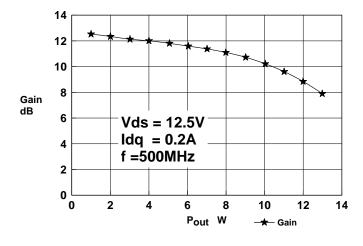


Figure 1 – Gain vs. Power Output.

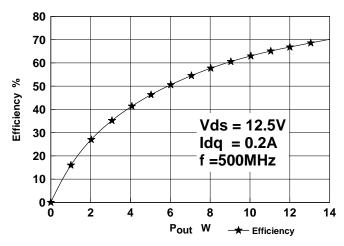


Figure 2 – Efficiency vs. Power Output.

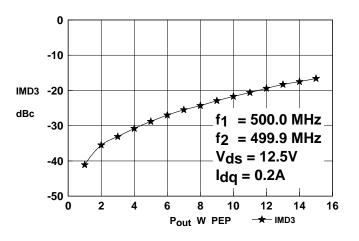


Figure 3 – IMD vs. Output Power.

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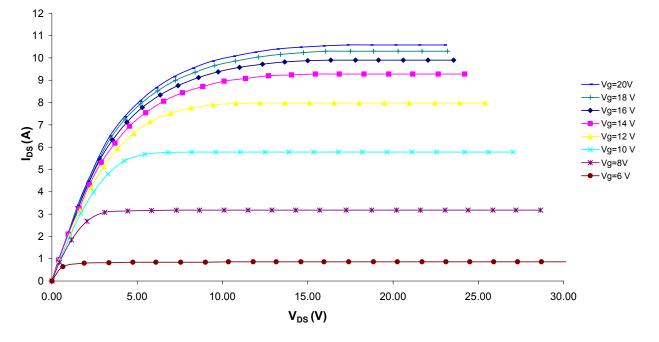
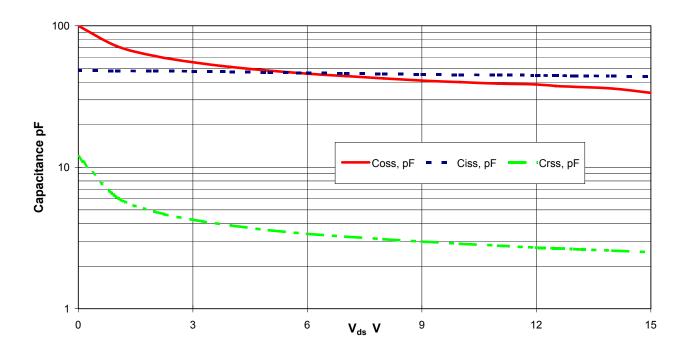


Figure 4 – Typical IV Characteristics.

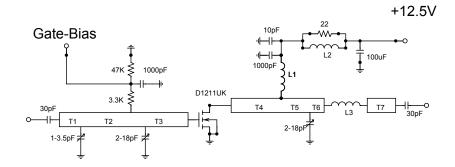




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D1211UK 500MHz TEST FIXTURE

Substrate 0.8mm PTFE/glass, Er=2.5

All microstrip lines W=1.5mm

- T1 6mm
- T2 35mm
- T3 16mm
- T4 11mm
- T5 7mm
- T6 7mm
- T7 23mm
- L1 6 turns 0.5mm dia enamelled copper wire, 4mm i.d.
- L2 1.5 turns 0.5mm enamelled copper wire on 2 hole ferrite core
- L3 1/16" dia wire hairpin loop 15mm long

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